

Appl. No. 10/034,717
Amdt. dated March 17, 2005
Reply to Office action of December 17, 2004

REMARKS/ARGUMENTS

Applicant has received the Office action dated December 17, 2004, in which the Examiner: 1) rejected claims 1-4, 6-7, 12-16, 21, 25 and 27 under 35 U.S.C. § 102(e) as being anticipated by Davis (U.S. Pat. No. 6,618,775); and 2) objected to claims 5, 8-11, 17-20, 22-24, 26 and 28-29 as being dependent upon a rejected base claim. In the Disposition of Claims, Applicant assumes the Examiner listed the allowed claims and the rejected claims incorrectly. Based on the arguments contained herein, Applicant respectfully requests reconsideration and allowance of the pending claims.

I. § 102 REJECTIONS

Claim 1, in part, requires "at least one on-chip logic device that stores data to said plurality of cache sets during normal operation." Claim 1 also requires "a logic gate that receives an enable signal when the on-chip logic analyzer is enabled, and which disables at least one of said plurality of said cache sets for storing data from said on-chip logic analyzer." Davis does not teach these limitations as suggested by the Examiner.

Davis teaches a system that monitors internal busses of a processor (see Abstract). Specifically, Davis teaches a circular buffer (662, 664 or 666) that continually stores data from a processor bus until a trigger signal is received. The trigger signal is asserted when a monitored event occurs (see col. 4, lines 36-49). After detecting a trigger, data is "retained in the circular buffer until it is uploaded to an external device or until the buffer is reset" (col. 4, lines 61-62).

The Examiner appears to equate the circular buffers taught in Davis with Applicant's claimed "cache sets." However, Davis does not teach or suggest that the circular buffers are cache sets. If the Examiner believes that cache sets are inherent to circular buffers, the Examiner is required to provide rationale or evidence tending to show inherency (see MPEP 2112). Also, "to establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described by the reference....Inherency, however, may not be established by probabilities or possibilities.'" *In re Robertson*, 169 F.3d 743, 745.

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Furthermore, Davis does not teach or suggest "[disabling] at least one of said plurality of said cache sets for storing data from said on-chip logic analyzer" as suggested by the Examiner. While Davis teaches storing data in a circular buffer, ceasing to store data in the circular buffer, exporting data from the circular buffer and resetting the circular buffer, Davis does teach or suggest disabling "cache sets for storing data from said on-chip analyzer" as required in claim 1. For at least these reasons, Applicant submits that claim 1 and all claims that depend from claim 1 are allowable.

Claim 12, in part, requires "a cache memory coupled to said CPU core, said cache memory including a plurality of cache sets that during normal operation store data written by the CPU core." Claim 12 also requires "at least one logic analyzer that receives information relating to the internal state of the processor, said logic analyzer being coupled to at least one of said plurality of cache sets, and wherein said logic analyzer is capable of gaining ownership of said at least one cache set to store selected portions of said received information when said on-chip logic analyzer is enabled." Davis does not teach these limitations as suggested by the Examiner.

Again, the Examiner appears to equate the circular buffers taught in Davis with the "cache memory including a plurality of cache sets" required in claim 12. Davis, however, does not teach or suggest that the circular buffers are part of "a cache memory" as required in claim 12. Also, the Examiner has provided no evidence or rationale tending to show inherency as is required (see MPEP 2112).

Furthermore, claim 12 requires that "at least one cache set" be used to "store data written by the CPU core" and to store "information relating to the internal state of the processor...when said on-chip logic analyzer is enabled." Davis does not teach or suggest that the circular buffer stores both "data written by the CPU core" and "information relating to the internal state of the processor...when [an] on-chip logic analyzer is enabled." Davis simply teaches that each circular buffer "stores data from a single processor bus" (see col. 3, lines 64-66). For at least these reasons, Applicant submits that claim 12 and all claims that depend from claim 12 are allowable.

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Claim 21, in part, requires "a CPU core coupled to said cache memory, said CPU core storing data to all operative cache sets during normal operation." Claim 21 also requires "an on-chip logic analyzer capable of receiving data reflecting the internal state of the processor, said on-chip logic analyzer coupled to at least one cache set, which is disabled from use by the CPU core when the on-chip logic analyzer is enabled." Davis does not teach or suggest these limitations as suggested by the Examiner.

Again, the Examiner incorrectly equates the circular buffers taught in Davis with the "cache memory" and "cache sets" required in claim 21. Davis does not teach or suggest that the circular buffers are cache memory and the Examiner has provided no evidence or rationale tending to show inherency as is required (see MPEP 2112).

Also, Davis does not teach or suggest "an on-chip logic analyzer capable of receiving data reflecting the internal state of the processor, said on-chip logic analyzer coupled to at least one cache set, which is disabled from use by the CPU core when the on-chip logic analyzer is enabled" as required in claim 21. While Davis teaches circular buffers, each storing data from a single processor bus, Davis does not teach or suggest "at least one cache set, which is disabled from use by [a] CPU core when [an] on-chip logic analyzer is enabled" as required in claim 21. For at least these reasons, Applicant submits that claim 21 and all claims that depend from claim 21 are allowable.

Claim 25, in part, requires "disabling a cache set from use by any device other than [an] on-chip logic analyzer." Again, the Examiner incorrectly equates a circular buffer taught in Davis with Applicant's claimed "cache set." Neither Davis nor the Examiner provides rationale or evidence tending to show a circular buffer is equal to a cache set. Furthermore, Davis does not teach or suggest "disabling a cache set from use by any device other than [an] on-chip logic analyzer" as required in claim 25. For at least these reasons, Applicant submits that claim 25 and all claims that depend from claim 25 are allowable.

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II. CONCLUSIONS

In the course of the foregoing discussions, Applicant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicant respectfully requests reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,



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